

CLAIMS

What is claimed is:

1. A method for optimally mapping a general set of resources to a specific integrated circuit design, comprising steps of:
 - abstracting sets of transistors into abstracted resources, said abstracted resources including at least one of a transformative resource, a coordinating resource, and a state management resource; and
 - utilizing a sea-of-platforms for unifying a flexible and malleable collection of said abstracted resources in such a way as to optimize said abstracted resources for a specific integrated circuit design.
2. The method of claim 1, wherein said transformative resource includes at least one of conversion and translation of data, modulation, calculation, and coding and decoding.
3. The method of claim 1, wherein said coordinating resource includes at least one of timing, synchronization, buffering, and caching.
4. The method of claim 1, wherein said state management resource includes at least one of control of non-volatile storage structures, and tree traversal capabilities.
5. The method of claim 1, wherein said utilizing step comprises implementing a plesiochronous signaling discipline in said sea-of-platforms.
6. The method of claim 1, wherein said utilizing step comprises using broken

symmetry to optimize said abstracted resources for said specific integrated circuit design.

7. The method of claim 6, wherein said broken symmetry is in at least one of a physical 3-dimensional space, a temporal space and a code space.

8. A system for optimally mapping a general set of resources to a specific integrated circuit design, comprising:

means for abstracting sets of transistors into abstracted resources, said abstracted resources including at least one of a transformative resource, a coordinating resource, and a state management resource; and

means for utilizing a sea-of-platforms for unifying a flexible and malleable collection of said abstracted resources in such a way as to optimize said abstracted resources for a specific integrated circuit design.

9. The system of claim 8, wherein said transformative resource includes at least one of conversion and translation of data, modulation, calculation, and coding and decoding.

10. The system of claim 8, wherein said coordinating resource includes at least one of timing, synchronization, buffering, and caching.

11. The system of claim 8, wherein said state management resource includes at least one of control of non-volatile storage structures, and tree traversal capabilities.

12. The system of claim 8, wherein said utilizing step comprises means for implementing a plesiochronous signaling discipline in said sea-of-platforms.

13. The system of claim 8, wherein said utilizing step comprises means for using broken symmetry to optimize said abstracted resources for said specific integrated circuit design.

14. The system of claim 13, wherein said broken symmetry is in at least one of a physical 3-dimensional space, a temporal space and a code space.

15. A computer-readable medium having computer-executable instructions for performing a method for optimally mapping a general set of resources to a specific integrated circuit design, said method comprising steps of:

abstracting sets of transistors into abstracted resources, said abstracted resources including at least one of a transformative resource, a coordinating resource, and a state management resource; and

utilizing a sea-of-platforms for unifying a flexible and malleable collection of said abstracted resources in such a way as to optimize said abstracted resources for a specific integrated circuit design.

16. The computer-readable medium of claim 15, wherein said transformative resource includes at least one of conversion and translation of data, modulation, calculation, and coding and decoding.

17. The computer-readable medium of claim 15, wherein said coordinating resource includes at least one of timing, synchronization, buffering, and caching.

18. The computer-readable medium of claim 15, wherein said state management resource includes at least one of control of non-volatile storage structures, and tree traversal capabilities.

19. The computer-readable medium of claim 15, wherein said utilizing step comprises implementing a plesiochronous signaling discipline in said sea-of-platforms.

20. The computer-readable medium of claim 15, wherein said utilizing step comprises using broken symmetry to optimize said abstracted resources for said specific integrated circuit design.

21. The computer-readable medium of claim 20, wherein said broken symmetry is in at least one of a physical 3-dimensional space, a temporal space and a code space.